REMARKS

Reconsideration and allowance of this application are respectfully requested. Claims 1, 6 and 7 have been amended. Claims 1-10 are now pending in the application. The rejections are respectfully submitted to be obviated in view of the remarks presented herein.

Rejection Under 35 U.S.C. § 103(a) – Applicant's Admitted Prior Art in view of Iliadis et al.

Claims 1-8 have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Applicant's admitted prior art in view of Iliadis et al. (U.S. Patent Number 5,742,606; hereinafter "Iliadis"). The rejection is respectfully traversed.

As a preliminary matter, Applicant notes that although claim 9 has not been indicated as being rejected under 35 U.S.C. § 103(a) (Office Action page 4), it appears that such was the Examiner's intention as evident on page 5 of the Office Action, which discusses claim 9.

Regarding amended claims 1 and 6, Applicant's claimed invention relates to a method and apparatus of switching, such as in an input buffer type packet switching equipment. An arbiter outputs a connection permission signal to one of M input line buffers based on connection request signals outputted from the M input line buffers, and also outputs a control signal to a switch. The connection permission signal is output, at a designated slower timing interval than a normal timing interval, to an input line buffer that outputs cells to an external output line whose output line rate is slower than a corresponding input line rate. The designated slower timing interval is a constant periodic rate which is slower than said corresponding input line rate, and the designated slower timing interval is set so that arrival of cells at the output line sections is at

a rate not greater than the output line rate (figure 4 and page 8, lines 11-17). Buffer overflow and output overflow are prevented in this switching system and method (page 7, lines 13-23).

Turning to the cited art, the background of the invention section of Applicant's specification describes an input buffer type packet switching equipment with FIFOs (404) provided in each of the input line buffers (402), and buffers (414) provided in each output line section (413). The buffers (414) are needed for transmission situations when an output line rate is slower than the corresponding input line rate.

Examiner maintains that the combination of Applicant's admitted prior art and Iliadis teaches each feature of the claimed invention. However, there is no teaching or suggestion in Applicant's figure 1 that "said designated slower timing interval is a constant periodic rate which is slower than said corresponding input line rate, said designated slower timing interval is set so that arrival of cells at said output line sections is at a rate not greater than said output line rate, and buffer overflow and output overflow are prevented," as Applicant claims.

Iliadis does not remedy the deficiencies of Applicant's figure 1. Iliadis teaches a switch for handling packet data traffic between a plurality of input and output ports. The data traffic fall into at least two different classes with different priorities and delay sensitivities. The switch has input ports with input queues and output ports with output queues. A control means detects an overflow state in the output queues, whereupon an interrupting means inhibits transmission of at least one class of traffic for a predetermined period T. The basic idea of Iliadis is to interrupt the transmission of data with a lower priority in favor of data having a higher priority directed to the same output port (column 4, lines 5-8). When the output buffer is completely filled and incoming packets are rejected, an overflow occurs. The interruption is then triggered and lasts

for the predetermined period T. The interruption time T can be any value up to the time taken to certainly empty the output buffer. In this way, the interrupting means delays a retry of transmission of a rejected low priority data packet for time period T. The time period T delay is triggered for each input line independently by an unsuccessful attempt to transmit a low priority packet (page 4, lines 37-44).

However, there is no teaching in Iliadis that "said designated slower timing interval is a constant periodic rate which is slower than said corresponding input line rate," as recited in Applicant's claims. Instead, Iliadis activates an interrupt of transmission of a packet. This interrupt is a delay in transmitting the packet, which lasts for a predetermined period of time T. Transmission of packets to the output buffer in Iliadis is resumed after the predetermined period T. This predetermined delay of transmission is only a delay of transmission for a predetermined period of time T, and is not a constant periodic rate for a connection permission signal, as claimed. Contrary to Applicant's slower timing interval, the delay of time period T is not a constant periodic rate, but only a single one-time delay period in which transmission is interrupted.

Additionally, Iliadis does not teach or suggest that "said designated slower timing interval is set so that arrival of cells at said output line sections is at a rate not greater than said output line rate, and buffer overflow and output overflow are prevented," as Applicant claims. An overflow condition is detected in Iliadis, upon which transmission is inhibited for the predetermined period T. The output buffers are already full before the overflow condition is detected and transmission inhibiting is initiated. Iliadis's system enters an overflow state every time an output buffer is full. Applicant's claimed invention is distinguished in that the

connection permission signal for switching cells is output to an input line buffer at a designated slower timing interval when the input line buffer outputs cells to an external output line whose output line rate is slower than a corresponding input line rate. In an exemplary embodiment of Applicant's invention, output buffers are even rendered unnecessary due to outputting cells to the external output line at a slower timing interval when that output line rate is slower than a corresponding input line rate, and no overflow occurs. At least by virtue of the aforementioned differences, the invention defined by Applicant's claims 1 and 6 are patentable over Applicant's figure 1 in view of Iliadis. Applicant's claims 2-5 are dependent claims including all of the elements of independent claim 1, which, as established above, distinguishes over Applicant's figure 1 in view of Iliadis. Therefore, claims 2-5 are distinguished over Applicant's figure 1 in view of Iliadis for at least the aforementioned reasons as well as for their additionally recited features. Reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) are respectfully requested.

Regarding claim 7, a method of outputting data in packet switching is described which stores data inputted from a plurality of input lines and selectively outputs the stored data to a plurality of external line sections. The stored data output to an external line section with an output line rate slower than a corresponding input line rate is outputted at a designated rate slower than the corresponding input line rate. The designated slower rate is a constant periodic rate which is slower than the corresponding input line rate, and the designated slower rate is set so that arrival of the outputted stored data at the external line sections is at a rate not greater than the output line rate. Buffer overflow and output overflow are also prevented.

As discussed above, neither Applicant's figure 1 nor Iliadis teach or suggest that "said designated slower rate is a constant periodic rate which is slower than said corresponding input line rate, said designated slower rate is set so that arrival of said outputted stored data at said external line sections is at a rate not greater than said output line rate, and buffer overflow and output overflow are prevented," as Applicant claims. At least by virtue of the aforementioned differences, the invention defined by Applicant's claim 7 is patentable over Applicant's figure 1 in view of Iliadis. Applicant's claims 8 and 9 are dependent claims including all of the elements of independent claim 7, which, as established above, distinguishes over Applicant's figure 1 in view of Iliadis. Therefore, claims 8 and 9 are distinguished over Applicant's figure 1 in view of Iliadis for at least the aforementioned reasons as well as for their additionally recited features. Reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) are respectfully requested.

Rejection Under 35 U.S.C. § 103(a) – Applicant's Admitted Prior Art in view of Iliadis et al. and further in view of Charny et al.

Claim 10 has been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Applicant's admitted prior art in view of Iliadis and further in view of Charny et al. (U.S. Patent Number 6,072,772; "Charny"). The rejection is respectfully traversed.

As discussed above, Applicant's figure 1 in view of Iliadis fails to teach or suggest that "said designated slower rate is a constant periodic rate which is slower than said corresponding input line rate, said designated slower rate is set so that arrival of said outputted stored data at said external line sections is at a rate not greater than said output line rate, and buffer overflow and output overflow are prevented," as recited in claim 7.

Charny does not remedy the deficiencies of Applicant's figure 1 in view of Iliadis. Charny teaches an input-buffered cross-bar switch implementing a crossbar arbitration scheme, as shown in figure 1. An arbiter (32) is responsive to scheduling of each per-output channel queue by a corresponding rate controller, to control the processing of queued cells in scheduled queues through the switch, at a speedup S equal to a number of phases per cell slot (column 3, line 58 to column 4, line 11). The arbiter (32) uses a specific maximal match computation to choose one of the scheduled per-output-channel queues from which a cell may be transmitted in each phase. Each rate scheduler runs a Rate controlled Smallest Eligible Finish Time First (RSEFTF) algorithm (column 4, lines 12-14). A deterministic delay is guaranteed and guaranteed rates are arbitrarily assigned to packet transmissions between input channels and output channels (column 4, lines 51-61).

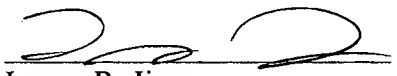
However, there is no teaching in Charny that "said designated slower rate is a constant periodic rate which is slower than said corresponding input line rate, said designated slower rate is set so that arrival of said outputted stored data at said external line sections is at a rate not greater than said output line rate, and buffer overflow and output overflow are prevented," as recited in Applicant's claim. Charny discusses only that cells are transferred between input and output channels with a plurality of queues of assigned rates. Queued cells are transferred by arbitration processing which includes performing a maximal match computation using timestamps. The combination of Applicant's figure 1 in view of Iliadis and further in view of Charny do not teach or suggest all elements as recited in Applicant's claim 7. At least by virtue of the aforementioned differences, the invention defined by Applicant's claim 7 is patentable over Applicant's figure 1 in view of Iliadis and further in view of Charny. Applicant's claim 10

is a dependent claim including all of the elements of independent claim 1, which, as established above, distinguishes over Applicant's figure 1 in view of Iliadis. Therefore, claim 10 is also distinguished over Applicant's figure 1 in view of Iliadis and further in view of Charny for at least the aforementioned reasons as well as for its additionally recited features. Reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) are respectfully requested.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



Lenny R. Jiang
Registration No. 52,432

SUGHRUE MION, PLLC
Telephone: (202) 293-7060
Facsimile: (202) 293-7860

WASHINGTON OFFICE
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